

The diagram illustrates the internal structure of a memory array. A **Row Address** is input to a **Row Decode** block, which outputs to the **wordlines** of the **RAM ARRAY**. A **Column Address** is input to a **Column Decode** block, which outputs to a **Column Select** block. The **Column Select** block is connected to the **Column Amplifiers** and the **I/O** port. The **RAM ARRAY** is a grid of **wordlines** and **bitlines**. A specific intersection is highlighted with a square, and a line connects it to the **Column Amplifiers**.

Figure 1A (Prior Art)

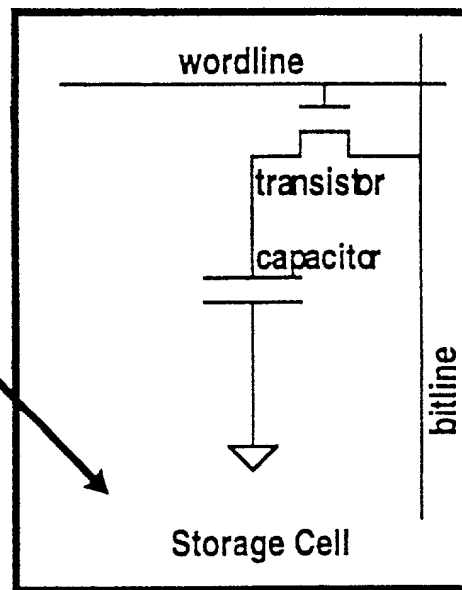


Figure 1B (Prior Art)

FIG. 2

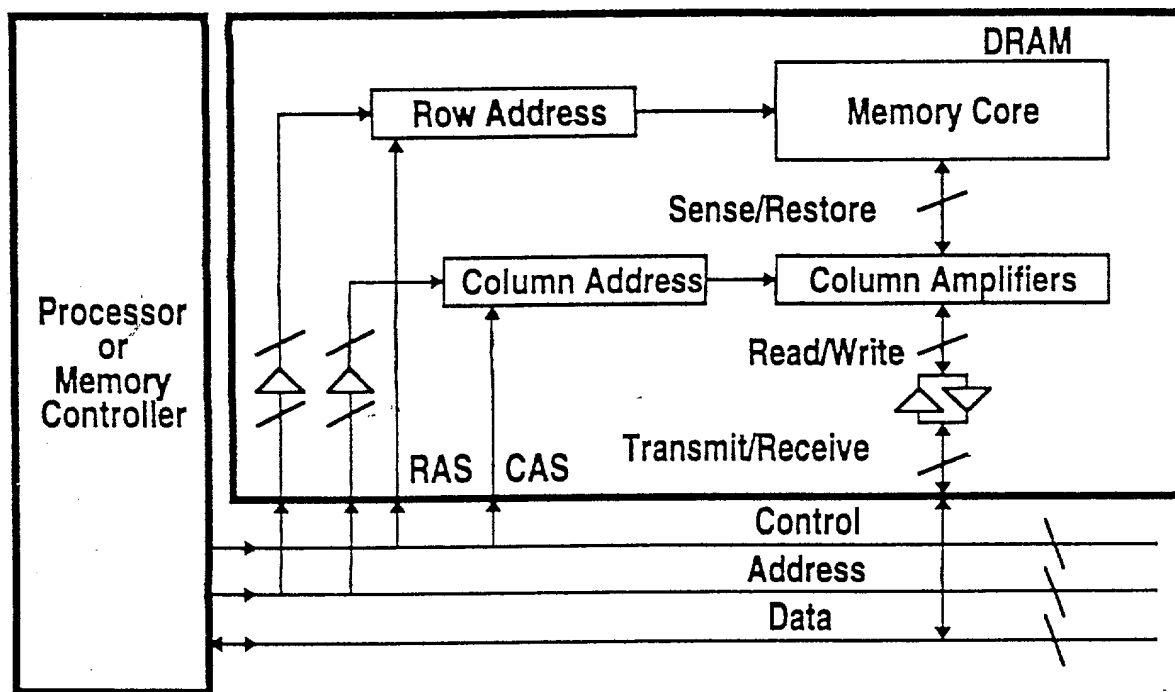


Figure 2
(Prior Art)

Figure 3A

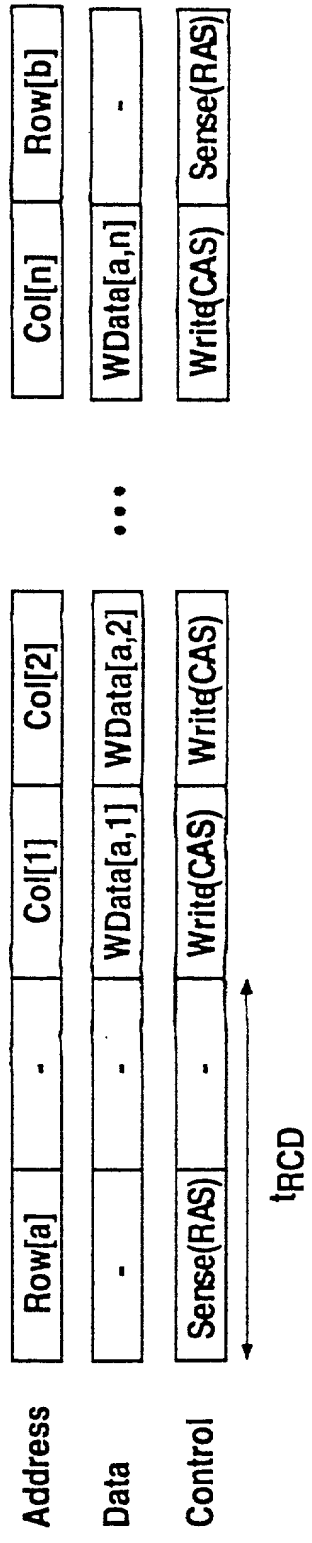


Figure 3A
(Prior Art)

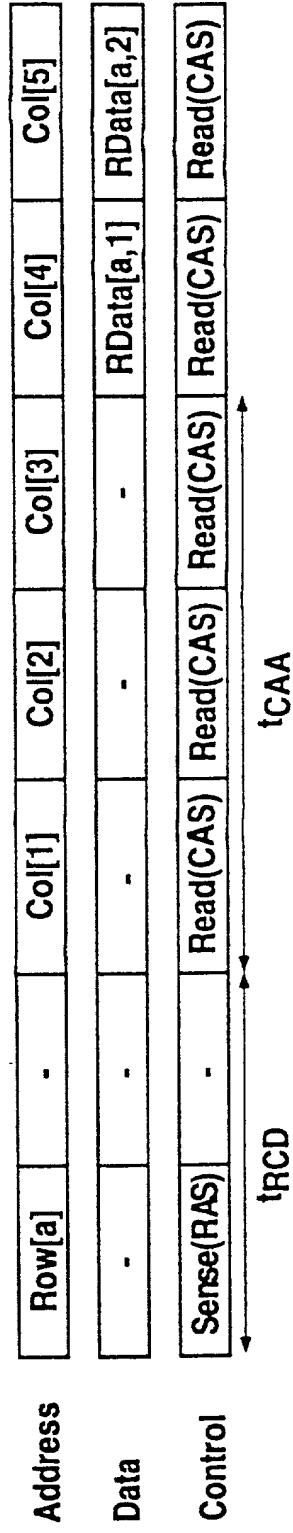


Figure 3B
(Prior Art)

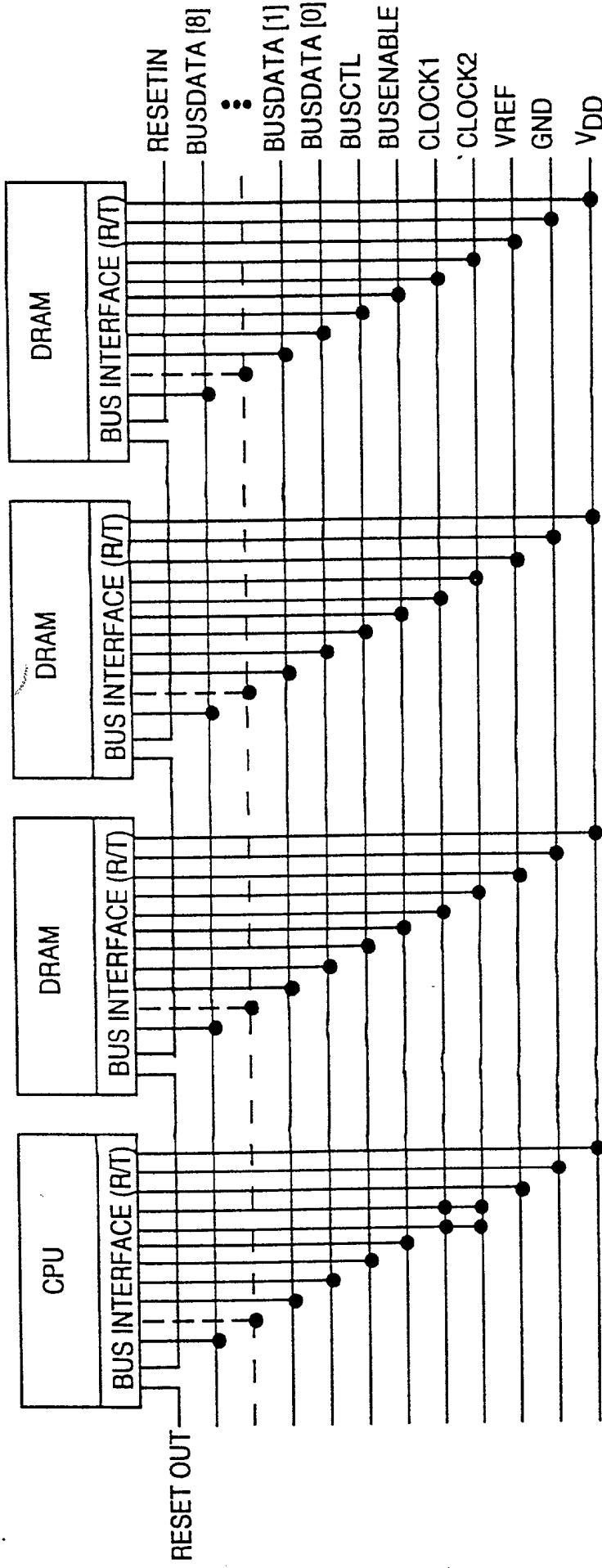


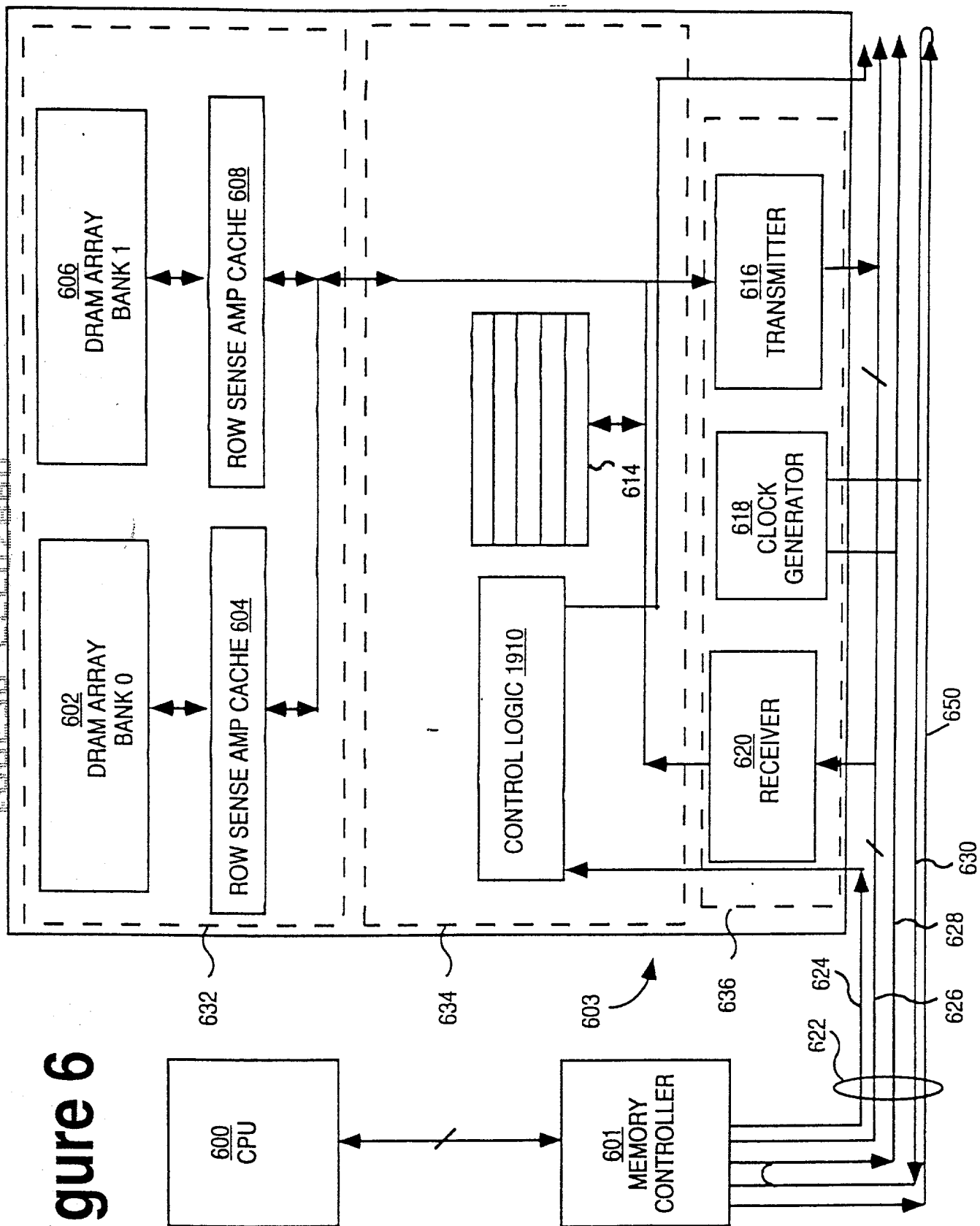
Figure 4
(Prior Art)

Clock Cycle	Bus-Enable	Bus-Ctrl	BusData											
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]			
OE	N	START	Op [0]	510			Adr [9:2]			502				
00	N	Op 514	Op [3]	512			Adr [17:10]			504				
1E	N	OpX [1]	516			Adr [26:18]			506					
10	N	Op [2]	518 520			Adr [35:27]			508					
2E	N	OpX [0]	U	U	Count [6,4,2]		522		U	U	U	U		
20	N	U	U	U	Count [7,5,3]		524		Count [1:0]		528		Adr [1:0]	501

500

Figure 5
(Prior Art)

Figure 6



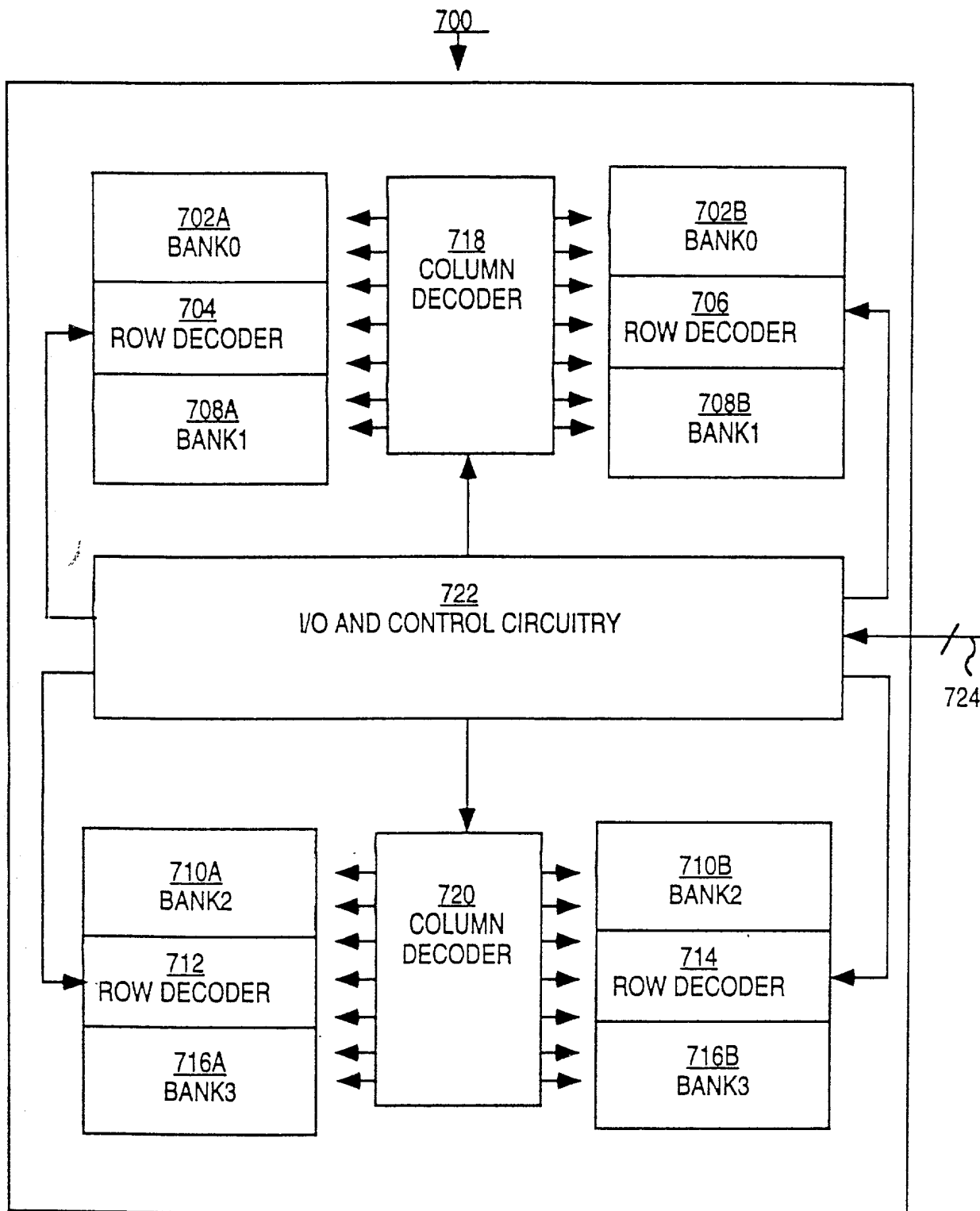


Figure 7

09370330.0330.2850

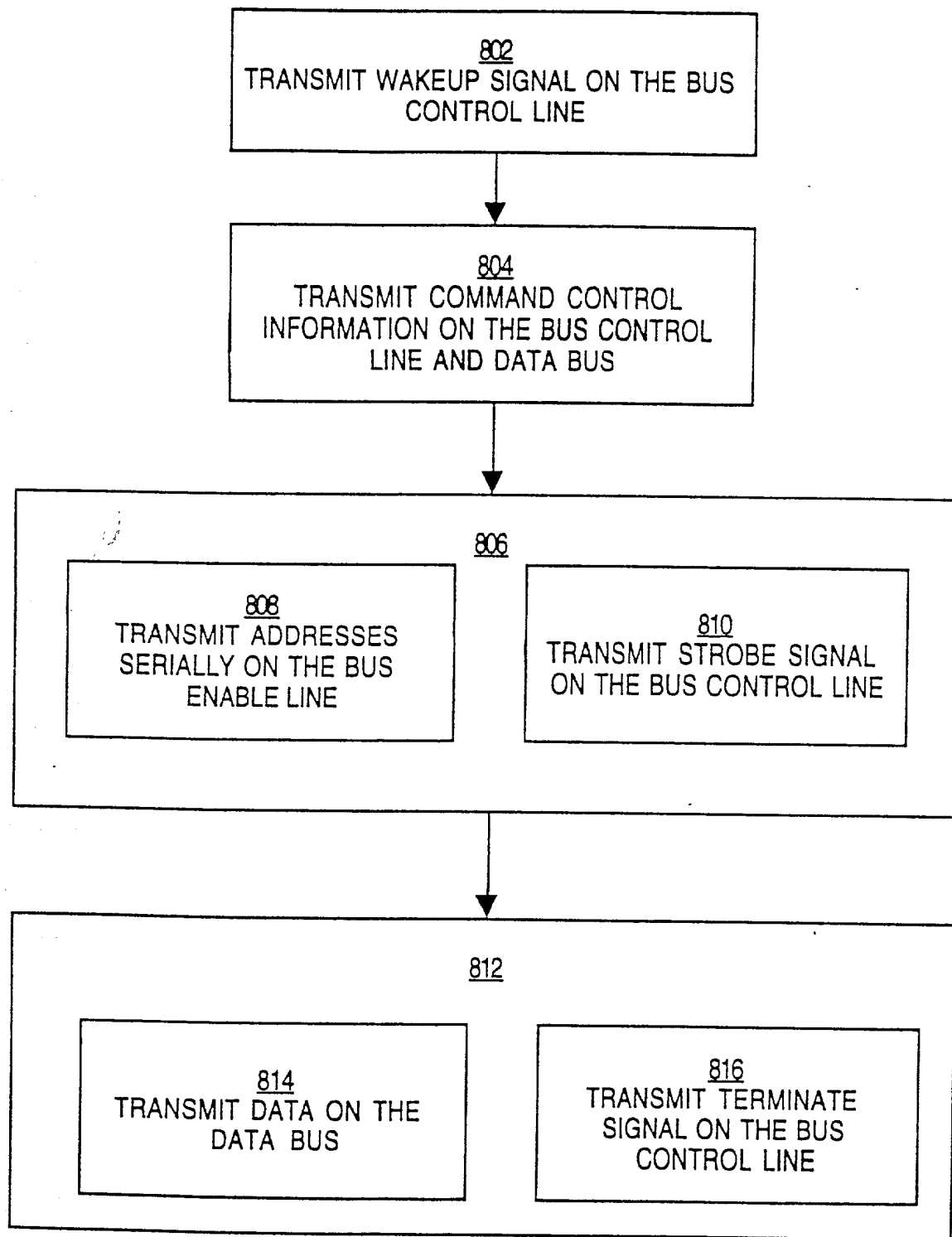


Figure 8

Clock Cycle	Bus-Enable	Bus-Ctrl	BusData									
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]:	
OE	N	START 902	Op[0] 'Write'		906		Adr [9:2]				904	
0O	N	Op[1] 'Reg' 908	Op[3] 'Bcst'		912		Adr [17:10]					
1E	N	OpX[1]	Adr [26:18]									
1O	N	Op[2] 'NoByteM' 910	Adr [35:27]									
2E	N	OpX[0]	U	U	U	EvalCC	Open	Close	Pend [2:0]			
2O	N	U	U	Mask [7:0];								

Figure 9

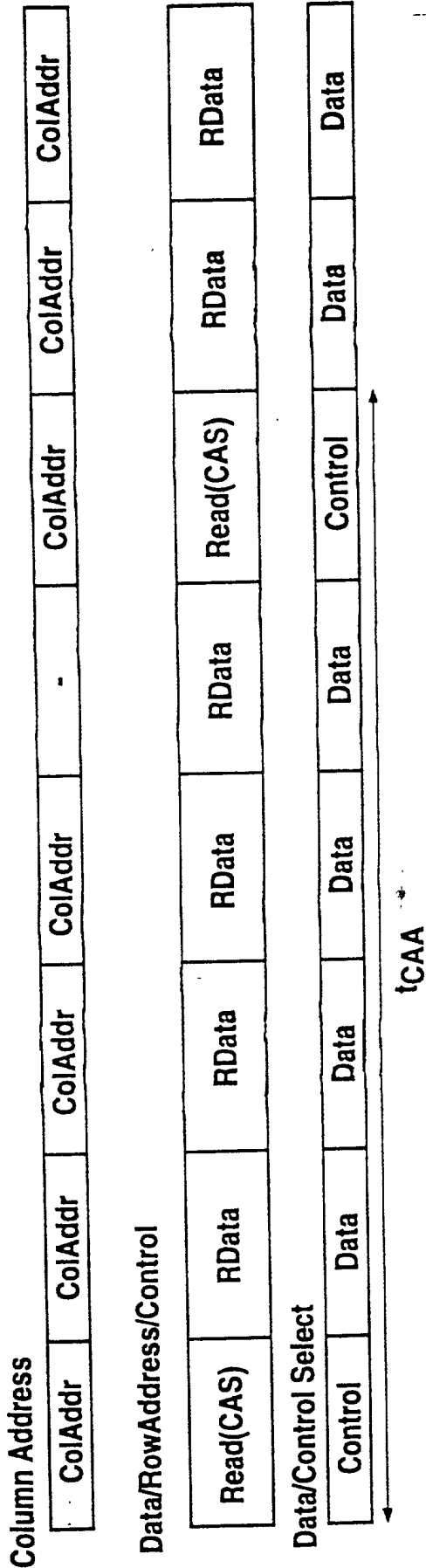


Figure 11
Prior Art

Figure 12

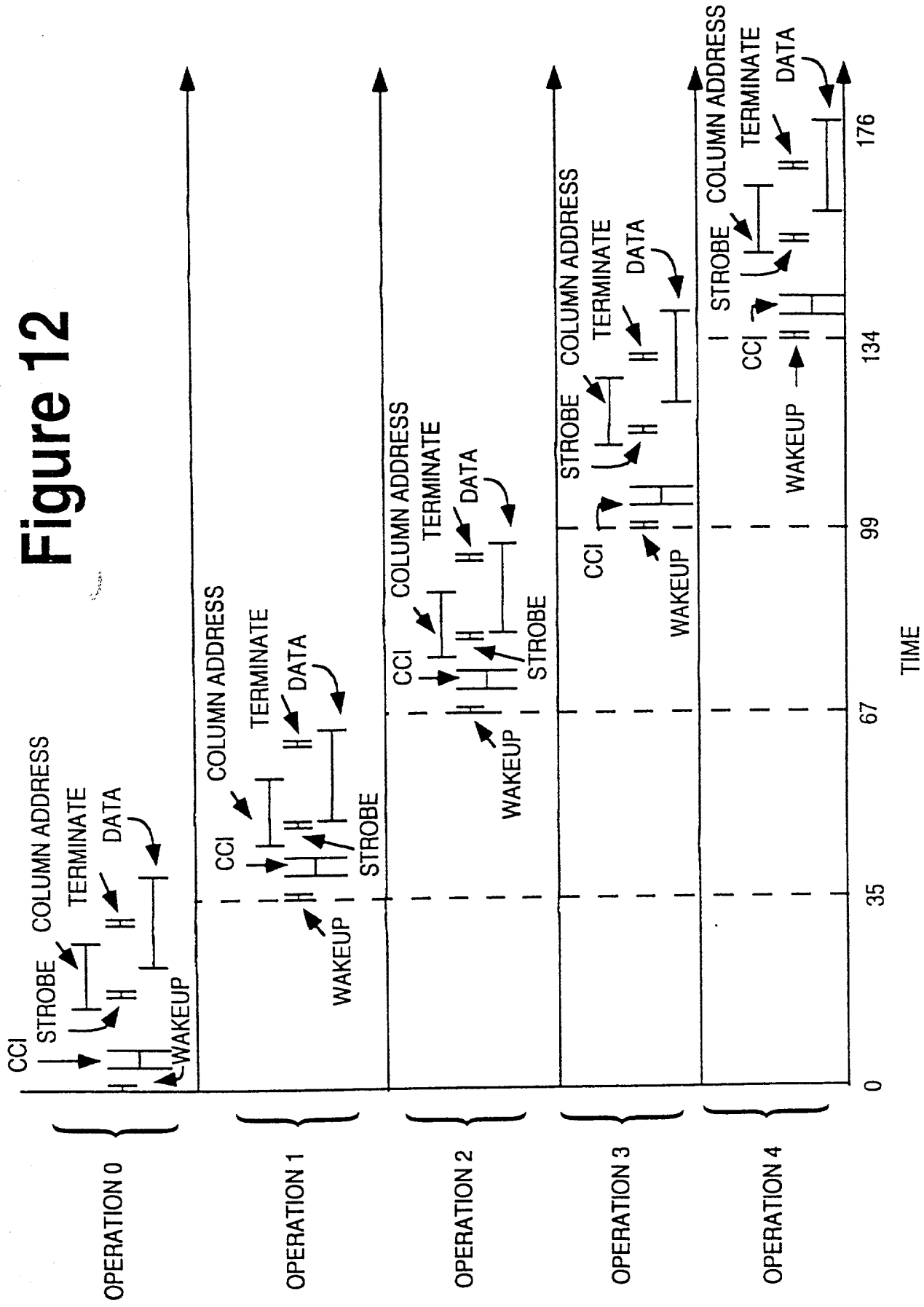
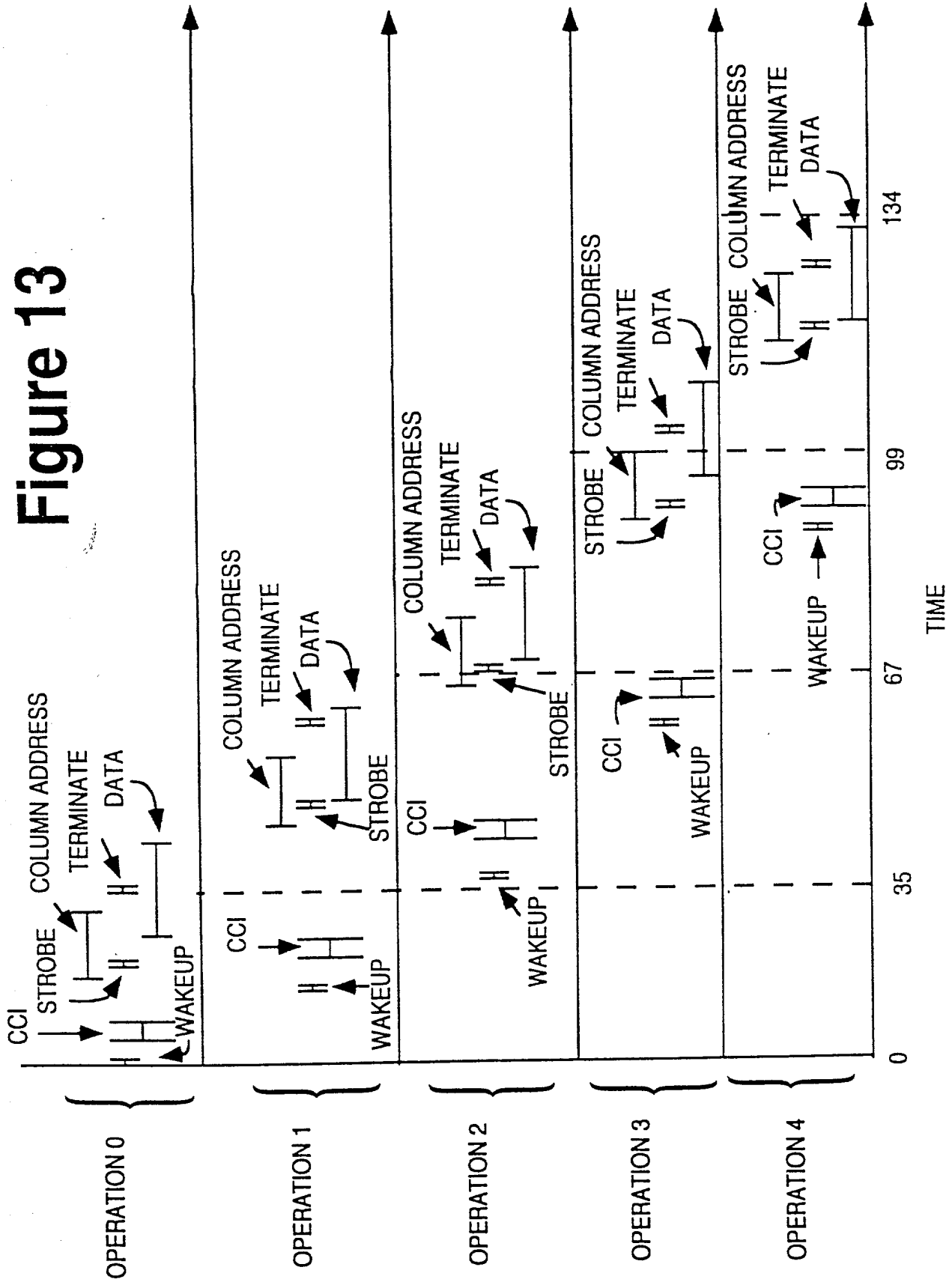


Figure 13



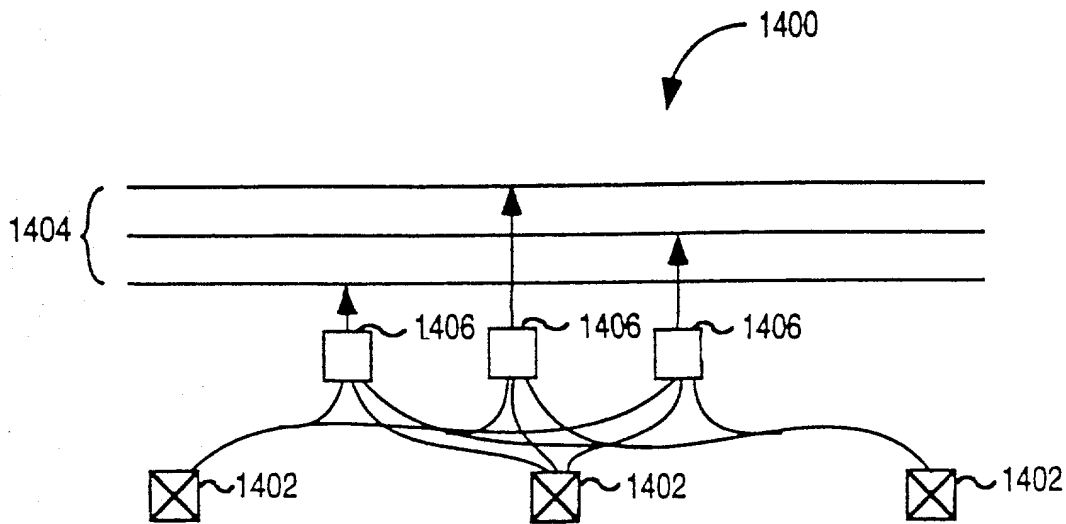


Figure 14
PRIOR ART

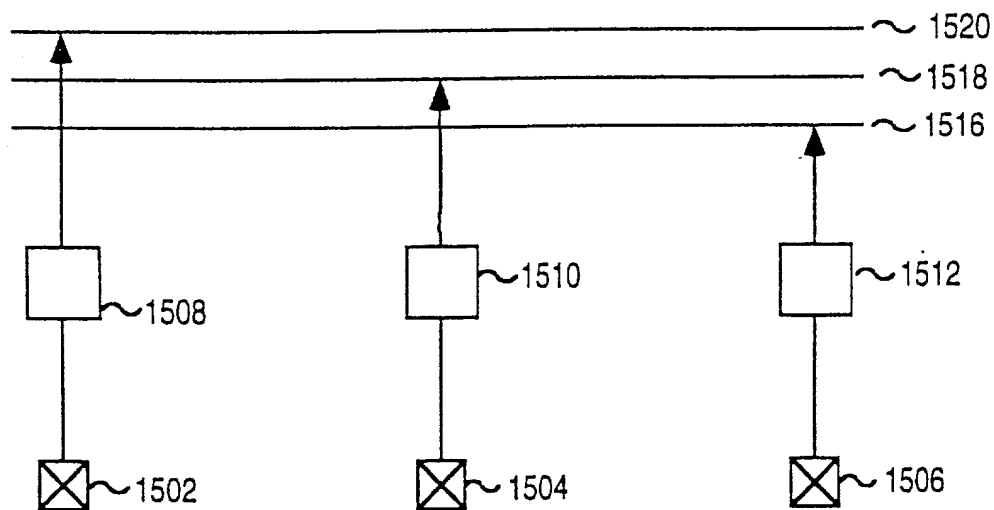


Figure 15

	Op[2] - NoByte M				Op[0] - Write		WriteOp		ReadRegOp		WriteRegOp		WregB	
	Op[3] - Bcst	Op[1] - Reg	Op[0] - Write	ReadOp	RegOp	RegOp	Rreg	Wreg						
ACTION														
ILLEGAL	0	0	0	0		X								
MEMORY WRITE DIRECTED BYTE MASK	0	0	0	1										
ILLEGAL	0	0	1	0										
ILLEGAL	0	0	1	1										
MEMORY READ DIRECTED	0	1	0	0	X									
MEMORY WRITE DIRECTED	0	1	0	1		X								
REGISTER READ DIRECTED	0	1	1	0	X		X	X	X					
REGISTER WRITE DIRECTED	0	1	1	1		X	X			X	X			
ILLEGAL	1	0	0	0										
MEMORY WRITE BROADCAST BYTE MASK	1	0	0	1		X								
ILLEGAL	1	0	1	0										
ILLEGAL	1	0	1	1										
ILLEGAL	1	1	0	0										
MEMORY WRITE BROADCAST	1	1	0	1		X								
ILLEGAL	1	1	1	0										
REGISTER WRITE BROADCAST	1	1	1	1		X	X			X			X	

Figure 16A

ACTION												
	MemOp	ReadMemOp	ReadMemDirectedOp	WriteMemOp	WriteMemNoByteMaskOp	WriteMemNoByteMaskDirectedOp	WriteMemNoByteMaskBroadcastOp	WriteMemByteMaskOp	WriteMemByteMaskDirectedOp	WriteMemByteMaskBroadcastOp	RsrvOp	BroadcastOp
ILLEGAL											X	
MEMORY WRITE DIRECTED BYTE MASK	X			X				X	X			
ILLEGAL											X	
ILLEGAL											X	
MEMORY READ DIRECTED	X	X	X									
MEMORY WRITE DIRECTED	X			X	X	X						
REGISTER READ DIRECTED												
REGISTER WRITE DIRECTED												
ILLEGAL											X	
MEMORY WRITE BROADCAST BYTE MASK	X			X				X		X		X
ILLEGAL											X	
ILLEGAL											X	
ILLEGAL											X	
MEMORY WRITE BROADCAST	X			X	X		X					X
ILLEGAL											X	
REGISTER WRITE BROADCAST												X

Figure 16B

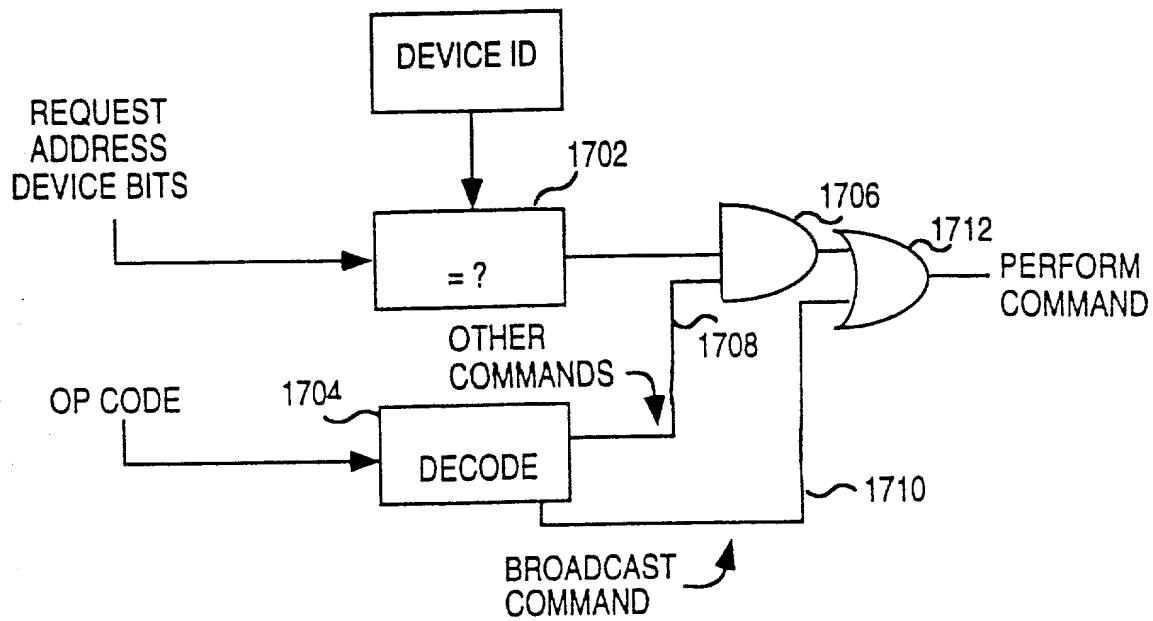


Figure 17

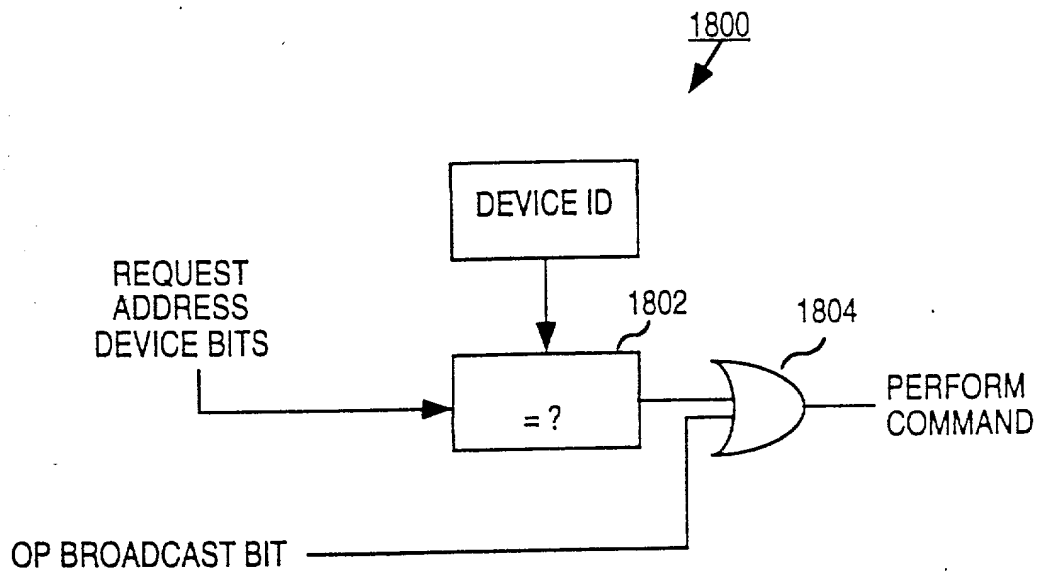


Figure 18

OPEN	CLOSE	PREVIOUS BANK STATE	NEW BANK STATE	ACTION
0	0	CLOSED	CLOSED	ILLEGAL
0	1	CLOSED	CLOSED	NO ACTION
1	0	CLOSED	OPEN	SENSE-CARD
1	1	CLOSED	CLOSED	SENSE-COMMAND-PRECHARGE
0	0	OPEN	OPEN	COMMAND
0	1	OPEN	CLOSED	COMMAND-PRECHARGE
1	0	OPEN	OPEN	PRECHARGE-SENSE-COMMAND
1	1	OPEN	CLOSED	PRECHARGE-SENSE-COMMAND-PRECHARGE

Figure 19

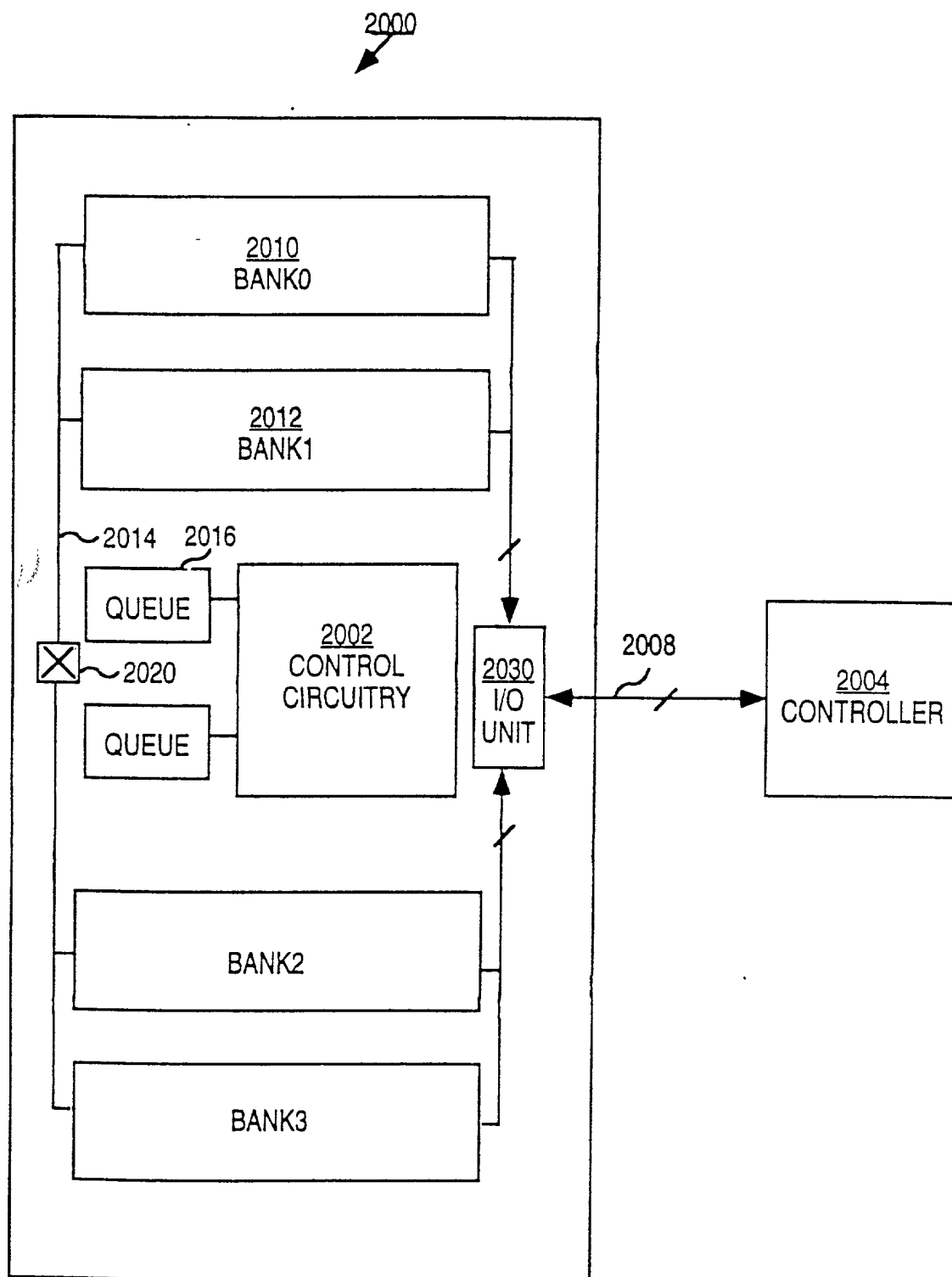
[illegible]

Figure 20A

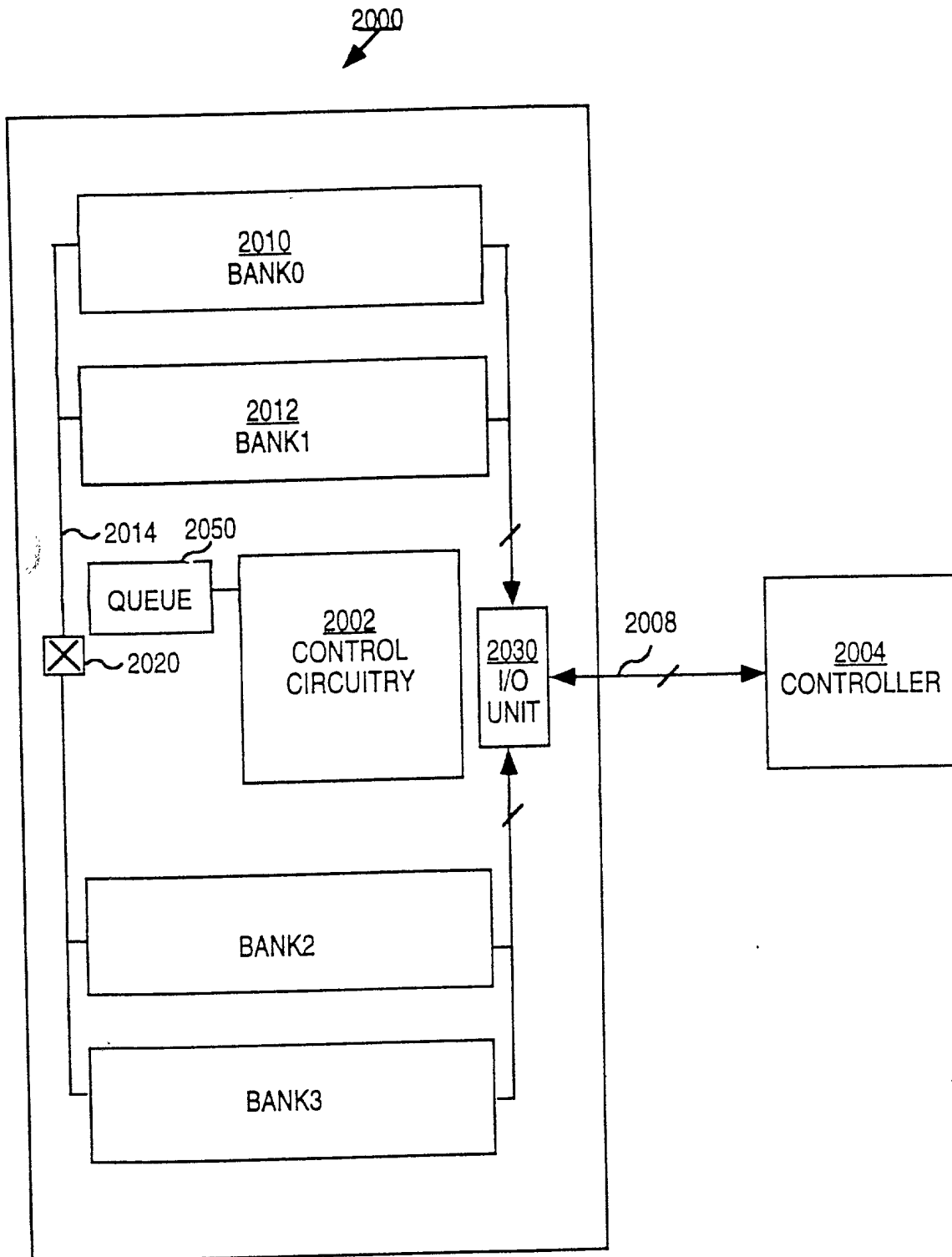


Figure 20B